Solutions – Midterm Exam

(October 21st @ 5:30 pm)
Clarity is very important! Show your procedure!

PROBLEM 1 (20 PTS)

- (5 pts) Complete the following table. The numbers are unsigned integers.

Decimal	BCD (bits)	Binary	Hexadecimal
181	0001 1000 0001	10110101	B5
59	01011001	00111011	3B
86	10000110	01010110	56
114	0001 0001 0100	01110010	72

- (5 pts) Complete the following table. The numbers are represented with 8 bits.

REPRESENTATION		
Decimal	**1's complement**	**2's complement**
-50	11001101	11001110
-109	10010010	10010011
77	01001101	01001101
-86	10101001	10101010

- (5 pts) Perform the following addition and subtraction of 8-bit unsigned integers. Indicate (every carry) or borrow from c_0 to c_8 (or b_0 to b_8). For the addition, determine whether there is an overflow. For the subtraction, determine whether we need to keep borrowing from a higher byte.

Example:

- 54 + 210

```
                c8=1 c7=1 c6=1 c5=1 c4=0 c3=1 c2=1 c1=0 c0=0
 54 = 0x36 =      0    0    1    1    0    1    1    0   +
210 = 0xD2 =      1    1    0    1    0    0    1    0
-------------------------------------------------------
Overflow! ->      1    0    0    0    0    1    0    0    0
```

- 77 - 194

```
                b8=1 b7=0 b6=0 b5=0 b4=0 b3=0 b2=1 b1=0 b0=0
Borrow out! ->
 77 = 0x4D =      0    1    0    0    1    1    0    1   -
194 = 0xC2 =      1    1    0    0    0    0    1    0
-------------------------------------------------------
                  0    0    0    0    1    0    1    1
```

- 86 + 181

```
                c8=1 c7=1 c6=1 c5=1 c4=0 c3=1 c2=0 c1=0 c0=0
 86 = 0x56 =      0    1    0    1    0    1    1    0   +
181 = 0xB5 =      1    0    1    1    0    1    0    1
-------------------------------------------------------
Overflow! ->      1    0    0    0    0    1    0    1    1
```

- 86 - 181

```
                b8=1 b7=0 b6=1 b5=0 b4=0 b3=0 b2=0 b1=1 b0=0
Borrow out! ->
 86 = 0x56 =      0    1    0    1    0    1    1    0   -
181 = 0xB5 =      1    0    1    1    0    1    0    1
-------------------------------------------------------
                  1    0    1    0    0    0    0    1
```

- (5 pts) Perform the following operations using the 2's complement representation with 8 bits. Determine whether the operations result in an overflow.

- -59 - 114

```
c8⊕c7=1                c8=1 c7=0 c6=0 c5=0 c4=1 c3=1 c2=0 c1=0 c0=0
Overflow!
-59 = 0xC5 =           1    1    0    0    0    1    0    1   +
-114 = 0x8E =          1    0    0    0    1    1    1    0
-------------------------------------------------------------
       0x53 =          0    1    0    1    0    0    1    1
```

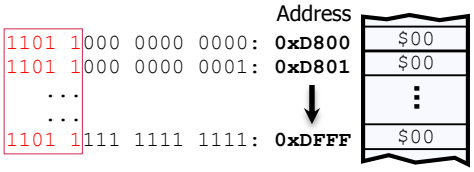
- -86 + 114

```
c8⊕c7=0                c8=1 c7=1 c6=1 c5=0 c4=0 c3=0 c2=1 c1=0 c0=0
No Overflow
-86 = 0xAA =           1    0    1    0    1    0    1    0   +
114 = 0x72 =           0    1    1    1    0    0    1    0
-------------------------------------------------------------
 28 = 0x1C =           0    0    0    1    1    1    0    0
```

PROBLEM 2 (10 PTS)

- A microprocessor has a 16-bit address line, where each address contains 8 bits. An SRAM device is connected to the microprocessor. The microprocessor has assigned the addresses `0xD800` to `0xDFFF` to this SRAM.
  - What is the size (in KB, or MB) of this SRAM?
  - What is the minimum number of bits required to represent the addresses only for this SRAM?

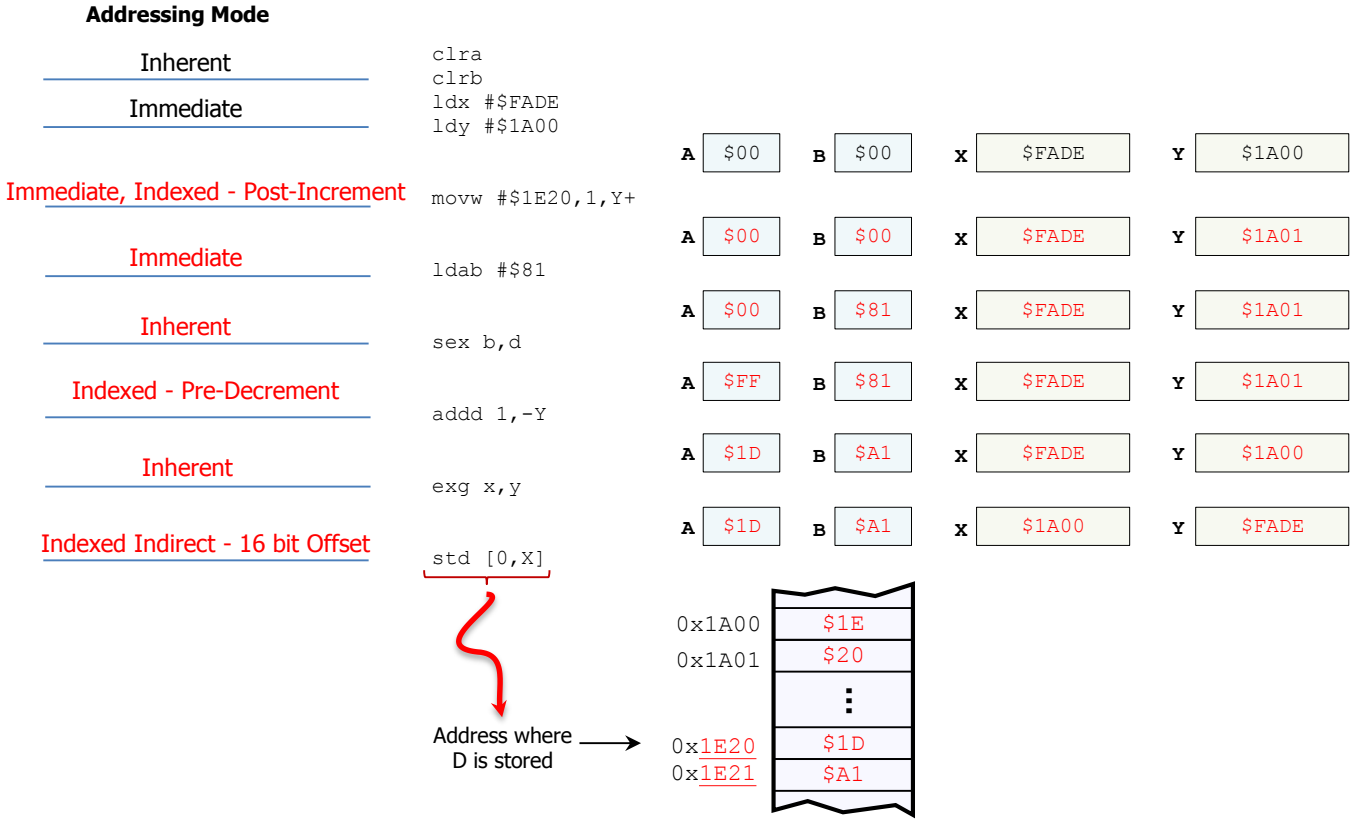
✓ The range `0xD800` to `0xDFFF` is akin to all possible cases with 11 bits. Thus the SRAM size is 2^{11} bytes = 1 KB.
✓ We only need 11 bits for this SRAM.



PROBLEM 3 (20 PTS)

Given the following set of instructions, complete the following:

- Register values (in hexadecimal format) as the instructions are executed.
- The state of the memory contents (in hexadecimal format) after the last instruction has been executed. Also, specify the memory address at which the contents of `D` are stored (last instruction).
- The addressing mode of each instruction. Be specific, if for example the addressing mode is indexed, indicate which one in particular. Note that the `movw` instruction uses two addressing modes.



PROBLEM 4 (10 PTS)

- Mark the correct option:
  - ✓ The Interrupt Vector Table contains the list of: Vector Addresses **Interrupt Vectors**
  - ✓ The Software Interrupt (`swi`) is a: Maskable Interrupt **Non-maskable Interrupt**

- Determine whether the following statements are True or False. If the statement is false, explain why.
  - ✓ Inside an Interrupt Service Routine, the values of the PC and CPU registers are pushed in the Stack.

    FALSE. The ISR does not do this. The processor does this before the ISR is executed.

  - ✓ An Interrupt Vector is the starting address of an Interrupt Service Routine.

    TRUE

  - ✓ When servicing a Reset, the values of the PC and CPU Registers are pushed in the Stack.

    FALSE. The processor does not save these registers, as the Reset will initialize these values.

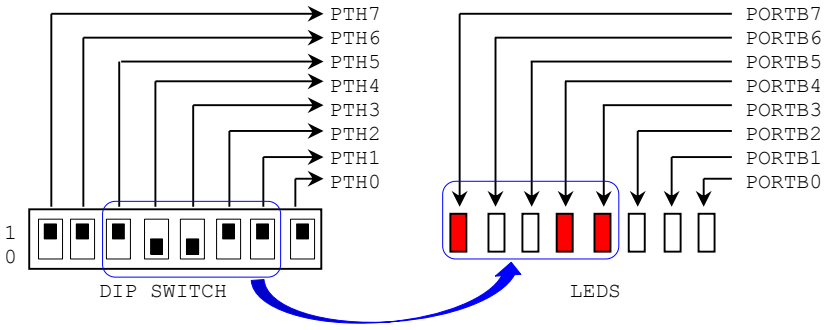
- Complete:
  - ✓ To enable/disable all maskable Interrupts, we configure the bit _**I**__ of CCR.

  - ✓ The `/XIRQ` Interrupt is enabled by setting the bit _**X**_ of CCR to 0.

PROBLEM 5 (20 PTS)

- (5 pts) Complete the Assembly Program below so that the state of bits 5 down to 1 on the DIP Switch is displayed only on the 5 leftmost bits on the LEDs (`PORT B`). The figure shows an example on the Dragon12-Light Board: the number `10011` is shown on the five leftmost LEDs, while the other LEDs are off.

```
ROMStart    EQU  $4000

; code section
            ORG   ROMStart

Entry:
_Startup:
            LDS   #$4000

            movb #$FF, DDRB
            movb #$00, DDRH


showDIPSW:  ldaa PTH

            ; /* Write instructions here */
```




```
anda #$3E
lsla
lsla
```

```
            ; /* End of your instructions */
            staa PORTB      ; Contents of register A are written on PORTB
            bra showDIPSW
```

- (5 pts) What is the time delay (in ms) that the following loop generates? Assume a 25 MHz bus clock. Consider that `pusha` takes 2 cycles, `pula` 3 cycles, `nop` one cycle and `dbne` 3 cycles.

```
ldx #56000
loop:  nop            ; 1 cycle
       nop            ; 1 cycle
       psha           ; 2 cycles
       pula           ; 3 cycles
       psha           ; 2 cycles
       pula           ; 3 cycles
       dbne X, loop   ; 3 cycles
```

$ntimes = 56000, n = 15$

$$n \times ntimes \times \frac{1}{25 \times 10^6} = 15 \times 56000 \times \frac{1}{25 \times 10^6} = \frac{33.6}{10^3}$$

$Time\ Delay = 33.6\ ms$

- (10 pts) After the `addd $10A0` instruction, what is the state of `D` and the following CCR flags: Z, C, V, and N? Does the `bcs next` instruction branches to '`next`'? Yes or no? Why?

```
       movw #$41AC, $10A0
       ldd #$730B
       addd $10A0
       bcs next
       ...
next:  ...
```

D

CCR: S X H I N Z V C

V = $c_{16} \oplus c_{15} = 1$
C = $c_{16} = 0$

	c_{16}=0	c_{15}=1	c_{14}=0	c_{13}=0	c_{12}=0	c_{11}=0	c_{10}=1	c_9=1	c_8=0	c_7=0	c_6=0	c_5=0	c_4=1	c_3=0	c_2=0	c_1=0	c_0=0	
0x730B =	0	1	1	1	0	0	1	1	0	0	0	0	1	0	1	1	+
0x41AC =	0	1	0	0	0	0	0	1	1	0	1	0	1	1	0	0	
0xB4B7 =	1	0	1	1	0	1	0	0	1	0	1	1	0	1	1	1	

- ✓ N flag: MSB of the result. N = 1
- ✓ C flag: Carry out of the summation. C = 0
- ✓ Z flag: Test whether the result is 0. Z = 0.
- ✓ V flag: Overflow when the operation is treated in 2's complement representation. V = 1

D: $B4B7

CCR: S X H I N Z V C = ■ ■ ■ ■ 1 0 1 0

- ✓ `bcs`: branch if carry set. Since C = 0, then `bcs next` DOES NOT branch to '`next`'.

PROBLEM 6 (20 PTS)

- Given the following Assembly code, specify the `SP` and the Stack Contents at the given times (right after the colored instruction has been executed). `SP` and the Stack Contents (empty) are specified for the first instruction (`LDS #$4000`).
- Specify a value in the instruction `adda` that would make the branch instruction `bvs` branch to `myloop`.